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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,647	07/09/2003	Hsilyn Huang	VIA-P003	3445
7590 01/12/2007 Fernandez & Associates, LLP PO Box D Menlo Park, CA 94026-6402		EXAMINER GEIB, BENJAMIN P ART UNIT 2181 PAPER NUMBER		
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MONTHS	01/12/2007	PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/616,647	HUANG ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 09 July 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-35 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 09 July 2003 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date: _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date <u>05/30/2006</u>	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

1. Claims 1-35 have been examined.
2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Application on 07/09/2003 and Information Disclosure Statement on 05/30/2006.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
4. Claims 1-35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
5. Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "pipeline" in claims 1, 6, 8-10, 16, 18, 19, 21, 24, 26, 27-29, 31 and 35 is used by the claims to mean a pipeline storage location, while the accepted meaning is "a sequence of functional units ('stages') which performs a task in several steps." (See FOLDOC definition of pipeline) The term is indefinite because the specification does not clearly redefine the term. The specification describes a plurality of

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“pipelines” (FIG. 2, components 209, 211, 213, 215, and 217) connected in a sequence, wherein the contents of each “pipeline” is passed to the next “pipeline” in the sequence according to the rising or falling edge of a clock (page 11, line 7 – page 12, line 12; FIG. 2). Thus, the specification appears to describe a single pipeline (the sequence of components in FIG. 2), according to the accepted meaning, wherein stages of the pipeline (FIG. 2, components 209, 211, 213, 215, and 217) are storage locations. These storage locations appear to the examiner to correspond to the claimed “pipelines”. Therefore, for the remainder of the examination, the term “pipeline” will be interpreted as “pipeline storage location”.

6. Claims 1-28 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: monitoring and controlling instruction dependency for microprocessors/microprocessor systems. The preambles of claims 1 and 19 state that each claim is a “method of monitoring and controlling instruction dependency” for microprocessors/microprocessor systems. However, the method steps for each claim do not refer to monitoring or controlling instruction dependency for microprocessors/microprocessor systems.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 1, 2, 11, and 19 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

9. Referring to claim 1, the claim recites a "method for monitoring and controlling instruction dependency for microprocessors" comprising steps of fetching, comparing, and verifying. These steps fail to provide a useful, concrete, and tangible result related to monitoring and controlling instruction dependency for microprocessors as indicated in the preamble. As such, the claim does not fall within any of the categories of patentable subject matter set forth in § 101 and is directed toward non-statutory subject matter.

10. Referring to claims 2 and 11, the claim depends upon claim 1, which fails to provide a useful, concrete, and tangible result as indicated above, and fails to further limit the invention such that a useful, concrete, and tangible result is provided. As such, the claim does not fall within any of the categories of patentable subject matter set forth in § 101 and is directed toward non-statutory subject matter.

11. Referring to claim 19, the claim recites a "method for monitoring and controlling instruction dependency for microprocessor systems". In all situations except for when both statements e) and e2) are true, the method comprising steps of fetching, receiving, comparing, and verifying. These steps fail to provide a useful, concrete, and tangible result related to monitoring and controlling instruction dependency for microprocessor systems as indicated in the preamble.

As such, the claim does not fall within any of the categories of patentable subject matter set forth in § 101 and is directed toward non-statutory subject matter.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 1-35 rejected under 35 U.S.C. 102(e) as being anticipated by Arnold et al., U.S. Patent No. 6,438,681 (Herein referred to as Arnold).

14. Referring to claim 1, Arnold has taught a method of monitoring and controlling instruction dependency for microprocessors, the method comprising:

fetching an instruction at a thread control element [*Instructions are received at the instruction dispersal unit (column 3, lines 13-23). Since these instructions (i.e. a thread) must be fetched, there is inherently a thread control element that fetches the instructions.*];

comparing one or more source operand identifications of the instruction to one or more temporary register identifications [*column 6, lines 50-66*], wherein each of the one or more temporary register identifications is stored in a

temporary register identification pipeline storage location of a set of one or more temporary register identification pipeline storage locations [*FIG. 3, components 87, 89, 91, and 93; column 6, lines 50-66*]; and

verifying whether any of the one or more source operand identifications matches any of the one or more temporary register identifications [*column 6, line 66 – column 7, line 10*].

15. Referring to claim 2, Arnold has taught the method of claim 1, wherein none of the one or more source operand identifications matches any of the one or more temporary register identifications [*column 6, line 66 – column 7, line 10*].

16. Referring to claim 3, Arnold has taught the method of claim 2, further comprising the step of initiating execution of the instruction [*column 3, lines 44-49*].

17. Referring to claim 4, Arnold has taught the method of claim 3, further comprising the step of verifying whether a destination operand of the instruction is a temporary register [*column 6, lines 35-66*].

18. Referring to claim 5, Arnold has taught the method of claim 4, wherein the destination operand is not a temporary register [*column 6, lines 35-66*].

19. Referring to claim 6, Arnold has taught the method of claim 5, further comprising the step of writing a null value into a first pipeline of the set of one or more temporary register pipeline storage locations [*Since register identifiers follow their associated instructions down the pipeline (column 6, lines 35-49), if the instruction doesn't have a register identifier then a null value is inherently written into the first latch (FIG. 2, component 87)*].

20. Referring to claim 7, Arnold has taught the method of claim 4, wherein the destination operand is a temporary register [*column 6, lines 35-66*].

21. Referring to claim 8, Arnold has taught the method of claim 7, further comprising the step of writing an identification corresponding to the destination operand into a first pipeline storage location of the set of one or more temporary register pipelines [*The register identifier (i.e. identification corresponding to the destination operand) of the instruction is written into the first latch (component 87) of the set of latches; See FIG. 3; column 6, lines 35-49*].

22. Referring to claim 9, Arnold has taught the method of claim 1, wherein the content in all except the last of the set of one or more temporary register pipeline storage locations is shifted to the next pipeline storage location at the beginning of each clock cycle [*column 6, lines 35-49*].

23. Referring to claim 10, Arnold has taught the method of claim 9, wherein the content of the last pipeline storage location of the set of one or more temporary register pipeline storage locations is released at the beginning of each clock cycle [*column 6, lines 35-49*].

24. Referring to claim 11, Arnold has taught the method of claim 1, wherein at least one of the one or more source operand identifications matches one of the one or more temporary register identifications [*column 6, line 66 – column 7, line 10*].

25. Referring to claim 12, Arnold has taught the method of claim 11, further comprising the step of prohibiting execution of the instruction [*If there is a match*

then a data dependency exists (column 6, line 66 – column 7, line 10) and the instruction is stalled (column 4, lines 15-19)].

26. Referring to claim 13, Arnold has taught the method of claim 12, further comprising the step of comparing the one or more source operand identifications to the one or more temporary register identifications at the beginning of each clock cycle until none of the one or more source operand identifications matches any of the one or more temporary register identifications [column 6, lines 50-66].

27. Referring to claim 14, Arnold has taught the method of claim 13, further comprising the step of verifying whether a destination operand of the instruction is a temporary register [column 6, lines 35-66].

28. Referring to claim 15, Arnold has taught the method of claim 14, wherein the destination operand is not a temporary register [column 6, lines 35-66].

29. Referring to claim 16, Arnold has taught the method of claim 15, further comprising the step of writing a null value into a first pipeline storage location of the set of one or more temporary register pipeline storage locations [*Since register identifiers follow their associated instructions down the pipeline (column 6, lines 35-49), if the instruction doesn't have a register identifier then a null value is inherently written into the first latch (FIG. 2, component 87)*].

30. Referring to claim 17, Arnold has taught the method of claim 14, wherein the destination operand is a temporary register [column 6, lines 35-66].

31. Referring to claim 18, Arnold has taught the method of claim 17, further comprising the step of writing an identification corresponding to the destination operand into a first pipeline storage location of the set of one or more temporary

register pipeline storage locations [*The register identifier (i.e. identification corresponding to the destination operand) of the instruction is written into the first latch (component 87) of the set of latches; See FIG. 3; column 6, lines 35-49.*]

32. Referring to claim 19, Arnold has taught a method of monitoring and controlling instruction dependency for microprocessor systems, the method comprising:

- a) fetching an instruction at a thread control element [*Instructions are received at the instruction dispersal unit (column 3, lines 13-23). Since these instructions (i.e. a thread) must be fetched, there is inherently a thread control element that fetches the instructions.*];
- b) receiving an instruction request at an arbiter, wherein the instruction request is issued from the thread control element [*Receiving an instruction at the instruction dispersal unit (FIG. 1, component 18); column 3, lines 13-23;*]
- c) comparing one or more source operand identifications of the instruction to one or more temporary register identifications [*column 6, lines 50-66*], wherein each of the one or more temporary register identifications is stored in a temporary register identification pipeline storage location of a set of one or more temporary register identification pipeline storage locations [*FIG. 3, components 87, 89, 91, and 93; column 6, lines 50-66*];
- d) verifying whether any of the one or more source operand identifications matches any of the one or more temporary register identifications [*column 6, line 66 – column 7, line 10*]; and

e) if none of the one or more source operand identifications matches any of the one or more temporary register identifications:

e1) verifying whether a destination operand of the instruction is a temporary register [*column 6, lines 35-66*]; and

e2) if the destination operand of the instruction is a temporary register: writing an identification corresponding to the destination operand into a first pipeline storage location of the set of one or more temporary register pipeline storage locations [*The register identifier (i.e. identification corresponding to the destination operand) of the instruction is written into the first latch (component 87) of the set of latches; See FIG. 3; column 6, lines 35-49*].

33. Referring to claim 20, Arnold has taught the method of claim 19, further comprising the step of initiating execution of the instruction [*column 3, lines 44-49*].

34. Referring to claim 21, Arnold has taught the method of claim 19, if the destination operand of the instruction is not a temporary register in step e2), further comprising the step of writing a null value into a first pipeline storage location of the set of one or more temporary register pipeline storage locations [*Since register identifiers follow their associated instructions down the pipeline (column 6, lines 35-49), if the instruction doesn't have a register identifier then a null value is inherently written into the first latch (FIG. 2, component 87)*].

35. Referring to claim 22, Arnold has taught the method of claim 19, if at least one of the one or more source operand identifications matches one of the one or

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more temporary register identifications in step e) [column 6, line 66 – column 7, line 10], further comprising the steps of:

prohibiting the execution of the instruction [*If there is a match then a data dependency exists (column 6, line 66 – column 7, line 10) and the instruction is stalled (column 4, lines 15-19)*];

reiterating step d) until none of the one or more source operand identifications matches any of the one or more temporary register identifications [column 6, lines 50-66]; and

verifying whether a destination operand of the instruction is a temporary register [column 6, lines 35-66].

36. Referring to claim 23, Arnold has taught the method of claim 22, wherein the destination operand is a temporary register [column 6, lines 35-66].

37. Referring to claim 24, Arnold has taught the method of claim 23, further comprising the step of writing an identification corresponding to the destination operand into a first pipeline storage location of the set of one or more temporary register pipeline storage locations [*The register identifier (i.e. identification corresponding to the destination operand) of the instruction is written into the first latch (component 87) of the set of latches; See FIG. 3; column 6, lines 35-49*].

38. Referring to claim 25, Arnold has taught the method of claim 22, wherein the destination operand is not a temporary register [column 6, lines 35-66].

39. Referring to claim 26, Arnold has taught the method of claim 25, further comprising the step of writing a null value into a first pipeline storage location of the set of one or more temporary register pipeline storage locations [*Since*

register identifiers follow their associated instructions down the pipeline (column 6, lines 35-49), if the instruction doesn't have a register identifier then a null value is inherently written into the first latch (FIG. 2, component 87)].

40. Referring to claim 27, Arnold has taught the method of claim 19, wherein the content in all except the last of the set of one or more temporary register pipeline storage locations is shifted to the next pipeline storage location at the beginning of each clock cycle [column 6, lines 35-49].

41. Referring to claim 28, Arnold has taught the method of claim 27, wherein the content of the last pipeline storage location of the set of one or more temporary register pipeline storage locations is released at the beginning of each clock cycle [column 6, lines 35-49].

42. Referring to claim 29, Arnold has taught a system for instruction dependency monitor and control, comprising:

a set of one or more thread control elements for fetching instructions
[Instructions are received at the instruction dispersal unit (column 3, lines 13-23). Since these instructions (i.e. a thread) must be fetched, there is inherently a thread control element that fetches the instructions.];

a set of one or more comparing elements [comparison logic; FIG. 3, component 24], wherein each of the one or more comparing elements is coupled to a corresponding thread control element in the set of one or more thread control elements [column 6, lines 50-66]; and

a set of one or more temporary register identification pipeline storage locations [latches; FIG. 3, components 87, 89, 91, and 93], wherein the one or

more temporary register identification pipeline storage locations are coupled to the one or more comparing elements [*column 6, lines 50-66*].

43. Referring to claim 30, has taught the system of claim 29, further comprising an instruction buffer [*latch (FIG. 3, component 56)*] coupled to the one or more thread control elements [*column 6, lines 35-49*].

44. Referring to claim 31, has taught the system of claim 30, further comprising an arbiter [*instruction dispersal unit; FIG. 1, component 18*], wherein the arbiter is coupled to the one or more thread control elements, the one or more comparing elements, and the one or more temporary register identification pipeline storage locations [See *FIGs. 1 & 3; column 3, lines 13-23*].

45. Referring to claim 32, has taught the system of claim 31, further comprising an arithmetic logic unit (ALU) [*pipeline; FIGs. 1 & 3, component 21*] coupled to the arbiter [*column 3, lines 13-32*].

46. Referring to claim 33, has taught the system of claim 32, further comprising a set of one or more input data buffers [*latch (FIG. 3, component 58)*] coupled to the arbiter, wherein each input data buffer corresponds to a thread control element of the one or more thread control elements [*column 6, lines 35-49*].

47. Referring to claim 34, has taught the system of claim 33, further comprising a set of one or more temporary register buffers [*the registers that are identified by the register identifiers*] coupled to the arbiter, wherein each temporary register buffer corresponds to a thread control elements of the one or more thread control elements [*column 6, lines 35-49*].

48. Referring to claim 35, has taught a system for instruction dependency monitor and control, comprising:

a set of one or more thread control elements for fetching instructions

[Instructions are received at the instruction dispersal unit (column 3, lines 13-23).

Since these instructions (i.e. a thread) must be fetched, there is inherently a thread control element that fetches the instructions.];

a set of one or more comparing elements [comparison logic; FIG. 3, component 24], wherein each of the one or more comparing elements is coupled to a corresponding thread control element in the set of one or more thread control elements [column 6, lines 50-66];

a set of one or more temporary register identification pipeline storage locations [latches; FIG. 3, components 87, 89, 91, and 93], wherein the one or more temporary register pipeline storage locations are coupled to the one or more comparing elements [See FIG. 3; column 6, lines 50-66], and

an arbiter [instruction dispersal unit; FIG. 1, component 18] coupled to the thread control elements, the comparing elements, and the temporary register pipeline storage locations [See FIGs. 1 & 3; column 3, lines 13-23].

Conclusion

49. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she

thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

50. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Torng, U.S. Patent No. 4,807,115, has taught detecting instruction dependencies using a dispatch stack.

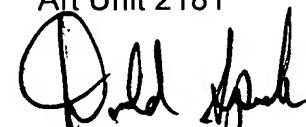
Arnold et al., U.S. Patent No. 6,643,762, has taught detecting instruction dependencies using a scoreboard.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181



DONALD SPARKS
SUPERVISORY PATENT EXAMINER